WHAT IS CLAIMED IS:

1. A semiconductor device comprising a plurality of signal terminals of a circuit block, wherein the signal terminals are arranged along a direction that intersects an extending direction of a wiring which is a wiring of an upper layer and outside the circuit block connected to the signal terminals, and wherein each of the signal terminals is arranged in the direction that intersects the extending direction outside the circuit block so that spaces for a plurality of wiring channels can be secured.

2. The semiconductor device according to claim 1, wherein a plurality of the circuit blocks are arranged along the extending direction of the wiring outside the circuit blocks and the signal terminals of each of the circuit blocks and the wiring outside the circuit blocks are electrically connected to each other.

3. The semiconductor device according to claim 2, wherein a wiring area is provided between a group of different circuit blocks among the circuit blocks.

4. The semiconductor device according to claim 1, wherein the signal terminal is extended in the direction that

intersects the extending direction of the wiring outside the circuit block.

5. The semiconductor device according to claim 1, wherein the plurality of the signal terminals are arranged along the extending direction of the outside-cell wiring and the position of the terminals for mutually adjoining signals along the extending direction of the outside-cell wiring are shifted to the direction that intersects the extending direction of the outside-cell wiring.

6. The semiconductor device according to claim 1, wherein the signal terminal is arranged in a frame of the circuit block.

7. The semiconductor device according to claim 1, wherein the signal terminal is constituted of a top wiring layer in the circuit block.

8. The semiconductor device according to claim 1, wherein a power supply terminal that extends to the direction that intersects the extending direction of the wiring outside the circuit block is provided in the frame of the circuit block.

9. The semiconductor device according to claim 8, the

power supply terminal is constituted of a top wiring layer in the circuit block.

10. A semiconductor device, wherein a power supply terminal of a circuit block is extended to the direction that intersects the extending direction of power supply wiring that is wiring of the upper layer and is connected to the power supply terminal, then extends the upper part of the circuit block.

11. The semiconductor device according to claim 10, wherein the power supply terminal is extended from end to end in the frame of the circuit block.

12. The semiconductor device according to claim 10, wherein the power supply terminal is constituted of the top wiring layer in the circuit block.

13. A semiconductor device, comprising:

a plurality of circuit blocks arranged along a first direction; and

a first wiring that extends to the first direction and electrically connects between the plurality of circuit blocks,

wherein a plurality of signal terminals are arranged

in each of the plurality of circuit blocks along a second direction that intersects the first direction;

wherein each of the plurality of signal terminals secures spaces for a plurality of wiring channels in the second direction; and

wherein the first wiring arranged on the wiring layer of the upper layer is electrically connected to each of the plurality of signal terminals.

14. The semiconductor device according to claim 13, each of the plurality of signal terminals is extended to the second direction.

15. The semiconductor device according to claim 13, wherein a plurality of each of the plurality of signal terminals are arranged along the first direction and the signal terminals that are mutually adjacent to the first direction are arranged, shifting the position to the second direction.

16. The semiconductor device according to claim 13, wherein each of the plurality of signal terminals is arranged in the frame of the circuit block.

17. The semiconductor device according to claim 13, wherein each of the plurality of signal terminals is

constituted of the top wiring layer in the circuit block.

18. The semiconductor device according to claim 13, wherein a power supply terminal that extends to the second direction is provided in the frame of the circuit block.

19. The semiconductor device according to claim 18, wherein the power supply terminal is constituted of the top wiring layer in the circuit block.

20. The semiconductor device according to claim 13, wherein the circuit block is a memory circuit, the first wiring constructs a wiring for an address signal, and the first wiring is connected in common to the circuit block.

21. The semiconductor device according to claim 13, wherein the circuit block is a memory circuit, the first wiring is wiring for data input, and the first wiring is connected in common to the circuit block.

22. The semiconductor device according to claim 13, wherein the circuit block is connected to wiring for a different clock signal.

23. The semiconductor device according to claim 1,

wherein the circuit block is a memory circuit and the signal terminal is formed on an input/output circuit area of the memory circuit.

24. A manufacturing method of a semiconductor device, comprising the steps of:

(a) arranging a plurality of circuit blocks along a first direction; and

(b) electrically connecting between the plurality of circuit blocks using first wiring that extends to the first direction,

wherein a plurality of signal terminals are arranged in each of the plurality of circuit blocks along a second direction that intersects the first direction;

wherein spaces for a plurality of wiring channels are secured in the second direction in each of the plurality of signal terminals; and

wherein the first wiring is arranged on the wiring layer of the upper layer than the signal terminal and electrically connected to the signal terminal.

25. A storage medium that stores data for designing an integrated circuit to be formed on a semiconductor chip,

wherein the data stored in the storage medium has data of a plurality of circuit blocks arranged along a first

direction and first wiring data that extends to the first direction and electrically connects between the plurality of circuit blocks;

wherein each of the plurality of circuit blocks has data of a plurality of signal terminals arranged along a second direction that intersects the first direction;

wherein each of the plurality of signal terminals has data in which spaces for a plurality of wiring channels are secured in the second direction; and

wherein data in the connected state between each of the plurality of signal terminals and the first wiring arranged on the wiring layer of the upper layer is provided.

26. The storage medium according to claim 25, comprising data arranged in the state in which each of the plurality of signal terminals is extended in the second direction.

27. The storage medium according to claim 25, comprising data in which each of the plurality of signal terminals is arranged along the first direction and the signal terminals that are mutually adjacent to the first direction are arranged, shifting the position to the second direction.

28. The storage medium according to claim 25,

comprising data in which each of the plurality of signal terminals is arranged in the frame of the circuit block.

29. The storage medium according to claim 25, wherein a semiconductor integrated circuit is designed using the storage medium.

30. The semiconductor device according to claim 14,

wherein the circuit block is a memory circuit, and

wherein the signal terminal is formed on the input/output circuit area of the memory circuit.

31. The semiconductor device according to claim 30, wherein the first wiring is a wiring for an address signal or a wiring for data.

32. The semiconductor device according to claim 24,

wherein the circuit block is a memory circuit, and

wherein the signal terminal is formed on the input/output circuit area of the memory circuit.

33. A semiconductor device, comprising:

a plurality of memory circuits arranged along a first direction; and

a plurality of first wiring that are electrically

connected to the plurality of memory circuits,

wherein a signal terminal is arranged in each of the plurality of memory circuits;

wherein the plurality of first wiring are formed on the wiring layer of the upper layer of the signal terminal, and extend over the terminal for the signal along the first direction;

wherein each of the signal terminals secures spaces for a plurality of wiring channels in a second direction that intersects the first direction; and

wherein each of the plurality of first wiring is arranged on a different wiring channel in the plurality of wiring channels and is electrically connected to the terminal for the different signal in the signal terminals of the plurality of memory circuits arranged in the first direction.

34. The semiconductor device according to claim 33, comprising:

a second wiring formed on the same layer wiring layer as the first wiring,

wherein the second wiring is electrically connected to each of the signal terminals of the plurality of memory circuits positioned on the same wiring channel.

35. The semiconductor device according to claim 33,

wherein the first wiring is a wiring for an address signal.

36. The semiconductor device according to claim 33, wherein the first wiring is a wiring for data.

37. The semiconductor device according to claim 33, wherein the first wiring is a wring for a clock signal.

38. The semiconductor device according to claim 33, wherein the signal terminal is formed on an input/output circuit area of the memory circuit.

39. The semiconductor device according to claim 34,

wherein the first wiring is one of wirings for the address signal and for the data; and

wherein the second wiring is the other of wirings for the address signal and for the data.

40. The semiconductor device according to claim 33, wherein in each of the memory circuit, a plurality of the signal terminals are arranged in the first direction and second direction, and the signal terminals adjacent to the first direction are arranged, shifting the position to the second direction.